SE/SEM III/CBSGS/ELEX/ED 12/5/16

QP Code : 30554

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. **1** is **compulsory** and Solve any **three** questions from remaining questions
(2) Assume suitable data wherever applicable.
(3) Draw neat and clean diagrams.

1. Answer any **four.** **20**
   (a) Justify that the space charge width increase with reverse biased voltage in a p-n junction diode.
   (b) Explain zener diode application as voltage regulator.
   (c) Define internal pinchoff voltage, pinchoff voltage and drain to source saturation voltage.
   (d) Describe construction and V-I characteristics of IGBT.
   (e) Explain two terminal MOS structure.

2. (a) Explain concept, working and characteristics of Tunnel diode. **10**
   (b) Explain the types of junction breakdown in case of zener diode. **10**

3. (a) For a n-channel JFET with I_{DSS} = 8 mA, V_P = -4 V **10**
      (i) If ID = 3mA calculate the value of V_{GS}
      (ii) Calculate $V_{DS\ (SAT)}$ for ID = 3mA
      (iii) Calculate transconductance (g_m)
   (b) Explain minority carrier distribution in BJT considering transistor in active, cut off and saturation mode. **10**

4. (a) Compare Enhancement type and Depletion type MOSFET on the basis of their construction, working principle, characteristics and biasing. **10**
   (b) Discuss construction and working of SCR with its characteristics in detail. **10**

5. (a) Discuss Ebers-Moll model for BJT in detail. **10**
   (b) Discuss HBT in detail. **10**

6. Write short notes **20**
   (a) Optocoupler
   (b) Gunn diode
   (c) MESFET
   (d) DIAC-TRIAC

SE/Sem III/ Elex/ CBSGS/ DCD

24/05/2016

QP Code : 30651

(3 Hours) **Total Marks: 80**

N.B.: (1) Question No. **1** is **compulsory**.

(2) Solve any **three** from remaining **five** questions.

(3) Draw neat **logic diagram** and assume **suitable data** wherever necessary.

Q 1 (a) Interfacing between CMOS and TTL 05

(b) Explain Shift Register and its applications

(c) PLA and PAL 05

(d) Draw truth table and logic diagram of Full Subtractor 05

Q 2 (a) Write a VHDL code for Full Adder 10

(b) Design MOD 8 asynchronous counter. 10

Q 3 (a) Design a mealy sequence detector to detect ---0101--- using D flip-flops and logic gates 10

(b) Design a circuit with optimum utilization of PLA to implement the following functions 10

$F1 = \sum m (0, 2, 5, 8, 9, 11)$

$F2 = \sum m (1, 3, 8, 10, 13, 15)$

$F3 = \sum m (0, 1, 5, 7, 9, 12, 14)$

Q 4 (a) Implement following function using 8:1 MUX and logic gates 10

$P (A,B,C,D) = \sum m (1,2,6,7,8,10,13,14)$

(b) Construct ring counter using IC 74194 and the output waveform 10

Q 5 (a) Use K-map to reduce following function and then implement it by NOR gates. 10

$F = \pi M (1, 2, 5, 8, 10, 12, 15) + d (0, 6)$

(b) Design 6 bit up counter using IC 74163, draw a circuit diagram and explain its working. 10

6. Write short notes on any **three** 20

i) JTAG and BIST

ii) Stuck at '0' and '1' faults

iii) XC 4000 FPGA architecture block diagram

iv) Noise Margins

SE sem III CBSGS Electronics CT 30/5/16

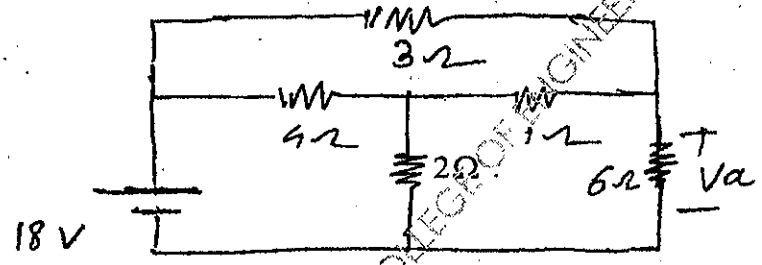
QP Code : 30699

(3 Hours) **[Total Marks : 80**

N. B. : (1) Question No. 1 is **compulsory.**
(2) Attempt any **three** questions from remaining questions.
(3) Use Smith chart wherever required.
(4) Assume suitable data if required.

1. (a) Test for following polynomial using continued fraction expansion only **20**
$P(s) = s^5 + 12s^4 + 45s^3 + 60s^2 + 44s + 48$
(b) Obtain transmission parameters (ABCD) in terms of z-parameters.
(c) List the types of damping in a series R-L-C circuit and mention the condition for each damping.
(d) Obtain S-domain (Laplace Transform) equivalent circuit diagram of an inductor and capacitor with initial condition.

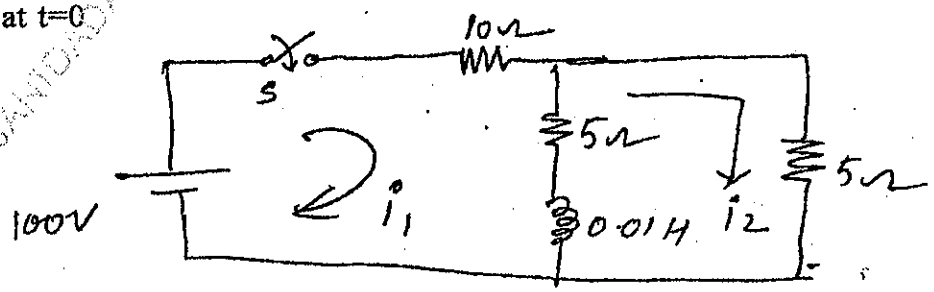
2. (a) Calculate voltage across the resister 6Ω using source shifting technique. **10**



(b) Compare and obtain Foster-I and Foster-II form using example of RC circuit **10**

$$Z(s) = \frac{(s+1)(s+6)}{s(s+4)(s+8)}$$

3. (a) Design a short circuit shunt stub match for Z_L=450 – 600j(Ω). For a line of Zo=300(Ω) and f = 20 MHz. Use Smith chart **10**
(b) In the circuit shown determine current I_1 and I_2 when switch is closed at t=0 **10**



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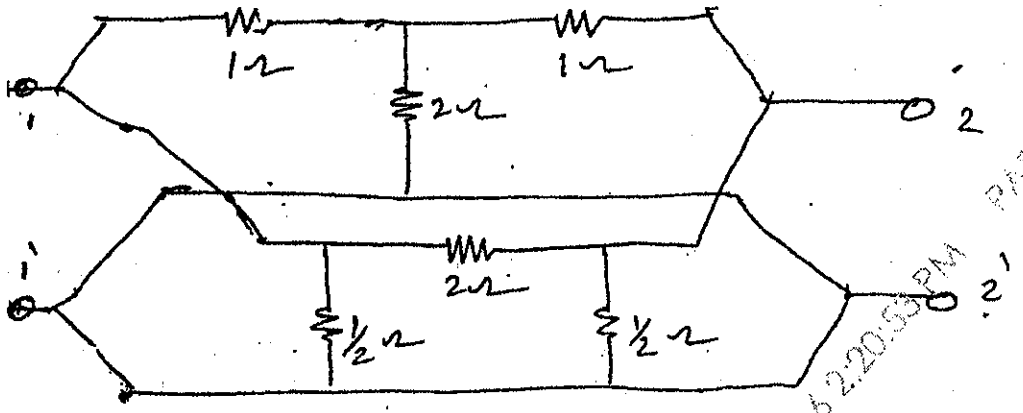
FW-Con. 11488-16.

4. (a) determine Y-parameter using interconnection of two port networks 10



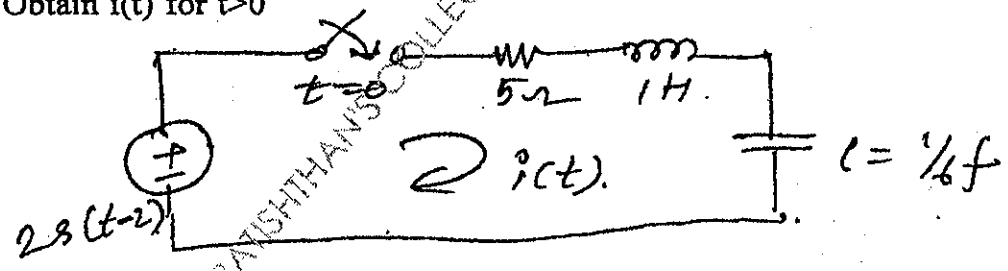
(b) Check for positive real function test 5

$$F(s)=\frac{2s^2+2s+1}{s^3+2s^2+s+2}$$

(c) Compare Cauer-I and Cauer-II form of LC network 5

$$Z(s)=\frac{2(s^2+1)(s^2+4)}{s(s^2+2)}$$

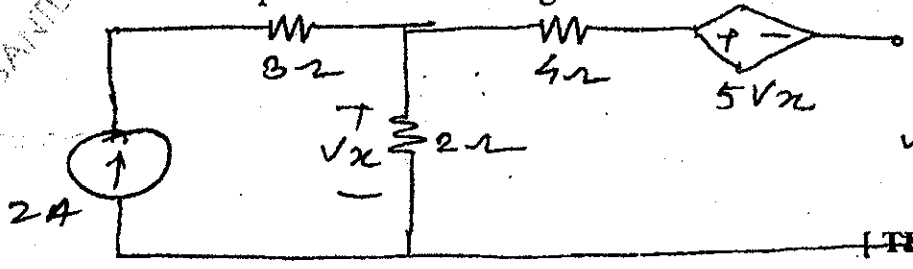
5. (a) Obtain i(t) for t>0 10



where r(t) is a ramp signal

(b) Derive an expression for characteritic equation of a transmission line. Also obtain 'α', 'β' and 'γ' of the line. 10

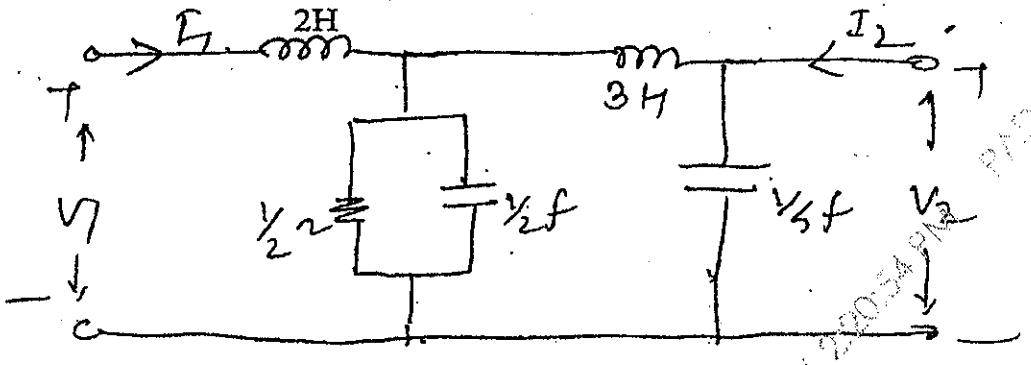
6. (a) Find Thevenin's equivalent of following n/w 8



[TURN OVER

(b) Explain various types of filters. 4

(c) Obtain $Z_{11}(s)$, $Z_{21}(s)$, $G_{21}(s)$ for the ladders n/w. 8



S.E /Sem III / Elex /GBSGS/ EIM 03/06/16. (7)

Q.P. Code: 30742

(3 Hours) Total Marks: 80

N.B. : (1) Question **No.1** is **Compulsory**.

(2) Attempt any **Three** questions from remaining **Five** questions.

1. Solve All (20)
   a) Define:- Accuracy, Precision, Linearity, Sensitivity, Resolution
   b) Write specifications of analog multimeter.
   c) Discuss the role of delay line in CRO.
   d) Explain selection criteria of transducers.

2. a. Explain in detail linear variable differential transformer. (10)
   b. Draw and explain multichannel data acquisition system. (10)

3. a. Discuss the working principle of RTD, Thermistor and Thermocouple. Also write their ranges and applications. (10)
   b. Draw and explain the Maxwell bridge. (10)

4. a. Draw and explain block diagram of CRO. (10)
   b. Write short note on "PC based instrumentation system". (10)

5. a. Explain the liquid level measurement using capacitive type method. (10)
   b. What is error? Write the classification of errors. Also discuss the methods to eliminate/reduce the errors during measurement. (10)

6. Write short notes on: (20)
   a. Wheatstone bridge
   b. Applications of DSO
   c. Resistance strain gauge
   d. Turbine flow meter

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FW-Con.12080-16.

SE|SEM IV|CBSGS|ELEX|DEC 13|5|16

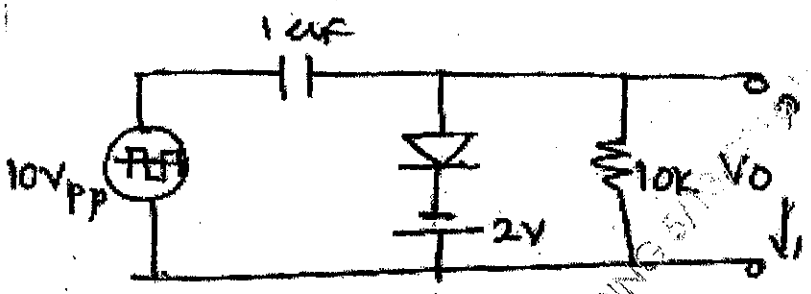
QP Code : 547800

(3 Hours) **[Total Marks : 80**

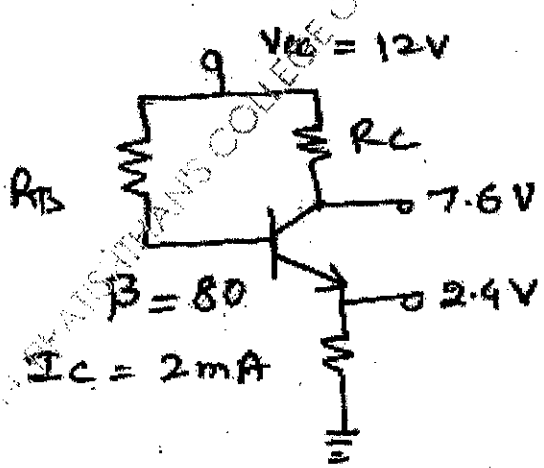
N.B. : (1) Question no. **1** is **compulsory** and solve any three out of remaining questions.
(2) Assume suitable data if necessary.

1. Solve any **five** **20**

(a) Identify the circuit and draw output waveform with proper voltage levels.



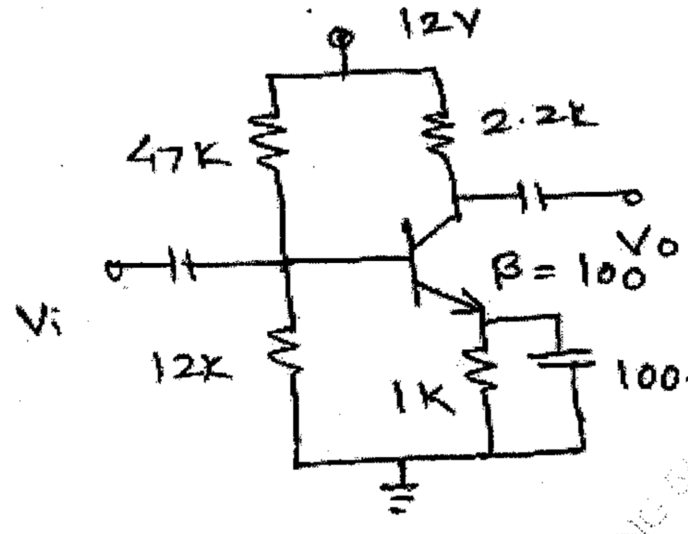
(b) Determine R_C and R_B for the following circuit. Assume VBE= 0.7V



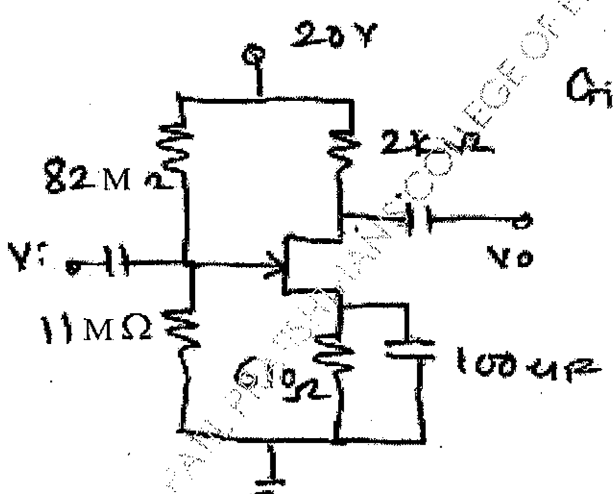
(c) Compare D-MOSFET and E-MOSFET Considering Construction and characterists.
(d) Explain working of Darlington connection and it's advantages.
(e) State and explain Bark hausen Criteria.
(f) Compare class A with Class AB power amplifier.

[TURN OVER]

2. (a) For the following circuit shown, find operating point and plot DC load line. **10**



(b) Determine A_V, Z_i and Z_o for the following circuit. **10**

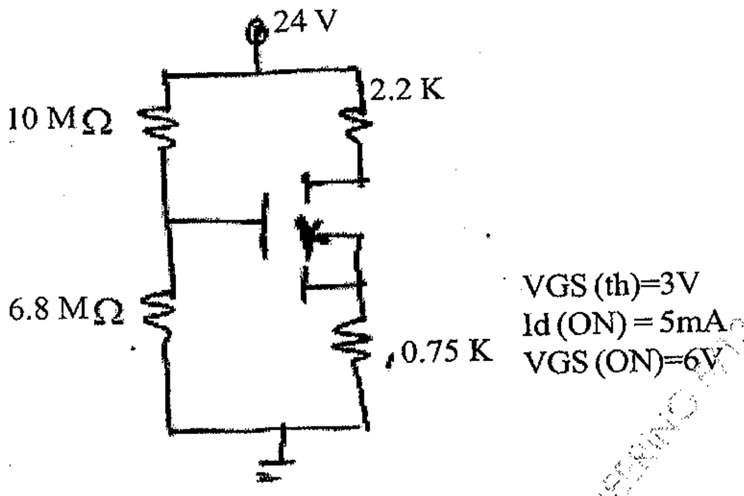


Given: $I_{DSS} = 12mA$
$V_P = -3V$
$r_d = 100k\Omega$
$g_{m0} = 8mS$

3. (a) Derive expression for overall voltage gain. Z_i and Z_o for two stage (CS-CS) amplifier. **10**
(b) Explain advantages of negative feedback and suggest scheme for improving i/p and o/p impedance of amplifier with proper explaination **10**

[TURN OVER]

4. (a) Derive expression for Ad, AC and CMRR for dual i/p - Balanced o/p differential amplifier. **10**
   (b) For the circuit shown, find Idq, V_{GSQ}, V_D and V_S **10**



5. (a) Explain working of class -B power amplifier, Derive expression for efficency. **10**
   (b) Explain high frequency analysis of CS amplifier. **10**

6. Write short notes on **20**
   (i) Hartley Oscillator
   (ii) Constant current Source in Differential amplifier
   (iii) Crossover distortion in class B
   (iv) Comparison of common Base and Common Emitter amplifier.

SE/SEMN/CBSGS/Elex/MAP 25/5/16

Q.P. Code : 548001

(3 Hours) Total Marks:80

N.B. 1) Question **number 1** is compulsory.
2) Attempt **any three** from remaining five questions.
3) Assume suitable data wherever necessary.
4) Figure to **the right** indicates full marks.

Q1. Attempt any four from the following (20)
a) At reset, interrupts in 8086 processor are disabled. Give reason.
b) List the differences between 8086 and 8088 processor.
c) Explain the feature of pipelining and queue in 8086 architecture.
d) Explain the significance of HOLD, RESET and READY signals in 8086 processor.
e) For 8086 op-code fetch machine cycle explain the significance of each T-state.

Q2)a) Classify and explain 8086 instruction set. (10)
b) Explain programmable interrupt controller 8259 – features and operation. (10)

Q3) a) Explain 8086-8087 coprocessor configuration in maximum mode of operation. (10)
b) Explain the following 8086 instructions (10)
a) CMPSB b) DIV AX c) LOOPE again d) REP SCASB e) XLATB

Q4) a) Write a detailed note on the interrupt structure of 8086 processor. (10)
b) Explain the need for DMA and modes of DMA data transfer. (10)

Q5) a) Explain the architecture of 8086 processor. What is the need for memory segmentation. (10)
b) With the help of a neat flowchart/algorithm write a program in 8086 assembly to arrange a set of ten 8-bit numbers initialized in data segment in ascending order. (10)

Q6) a) Write a brief note on programmable peripheral interface (PPI) IC – 8255 and its modes of operation. (10)
b) Using string instructions write a program in 8086 assembly to copy a block of ten bytes initialized in data segment to extra segment. Assume the necessary details. (10)

SE/Elex/Sem IV/CBSGS/PCS 31/05/2016

Q.P. Code : 548101

(3 Hours) [Total Marks : 80

N.B: 1. Question No. 1 is Compulsory.
2. Attempt **any three** from the remaining questions.
3. Assume suitable data wherever necessary.
4. Figure to right indicate full marks.

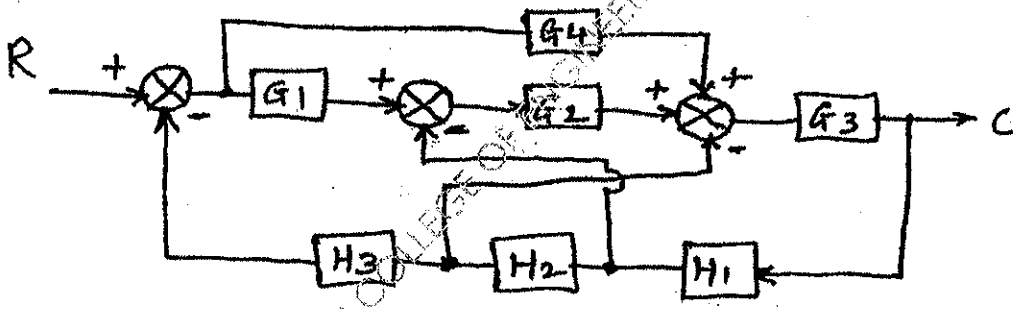
1. Attempt **any four** questions:- (20)

a) Explain Adaptive control system.
b) Explain lead and lag compensator.
c) Explain Controllability and Observability with its necessity condition for stability.
d) Determine whether the following systems are stable, marginally stable, and unstable

(i) -2,0; (ii) -2+j, -2-j; (iii) -2+j4, -2-j4, -2; (iv) $x(t) = \cos\omega t$; (v) $x(t) = e^{-t} \sin 4t$.

e) Examine the stability of $s^5 + 2s^4 + 2s^3 + 4s^2 + 4s + 8 = 0$ using Routh's method.

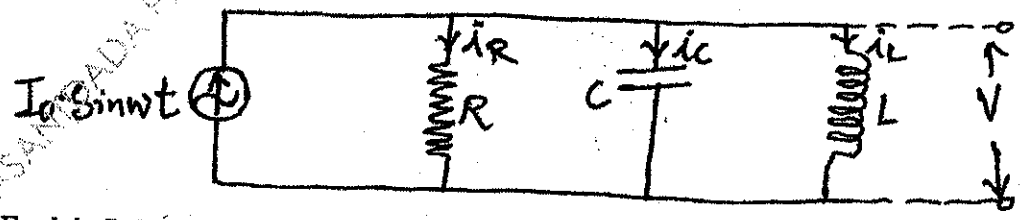
2. a) Obtain the overall transfer function from block diagram. (10)



b) Sketch the complete root locus for the system (10)

$$G(s)H(s) = [K(s+1)(s+2)] / [(s+0.1)(s-1)], \quad \text{where } K > 0.$$

3. a) Obtain the state variable model of the parallel RLC network. (10)



b) Explain P, PI and PID controller. (10)

TURN OVER

4. a) The state equation of a linear time-invariant system is given below: (10)

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -2 & 0 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u$$

Where $u > 0$.

Determine the following:

(i) The state transition matrix.

(ii) Controllability of the system.

b) Sketch the bode plot for the open loop transfer function given by: (10)

$G(s) = [288\ (s+4)] / [s(s+1)\ (s^2 + 4.8s + 144)]$ and $H(s) = 1$.

5. a) Derive the expressions of Peak Overshoot when step input applied to the system. (05)

b) Sketch the polar plot of $G(s) = 12 / [s(s+1)]$. (05)

c) For $G(s)H(s) = 1+4s / [s^2\ (1+s)(1+2s)]$, draw the Nyquist plot and examine the stability of the system. (10)

6. Attempt **any two-** (20)

a) Write a short note on Robust control system.

b) Construct the signal flow graphs for the following set of equations:

$$Y_2 = G_1Y_1 - G_2Y_4$$
$$Y_3 = G_3Y_2 + G_4Y_3$$
$$Y_4 = G_5Y_1 + G_6Y_3$$

where Y_4 is the output.

Using Mason's gain formula find the transfer function of the system.

c) Explain the Correlations between time and frequency domain specifications of the system.

SE Sem IV CBSGS Electronics FCE 6/6/16

QP Code : 548202

(3 Hours) **[Total Marks : 80**

N.B.: (1) Question No.1 is **Compulsory.**
(2) Attempt any **three** questions out of remaining **five** question.
(3) Assume suitable data if required.

1. Answer the following **(Any four):-**
   (a) Explain the concept of equivalent noise temperature. **5**
   (b) Explain the distortions in diode detector in AM receiver. **5**
   (c) Explain noise triangle concept in FM. **5**
   (d) Explain the sampling theorem & aliasing error. **5**
   (e) Explain the need of Modulation in analog communication. **5**

2. (a) Explain the direct and indirect method of generation of FM signal. **10**
   (b) Explain the different method of generation of SSB. **10**

3. (a) In superheterodyne receiver having no RF amplifier. the loaded Q of the antenna coupling circuit is 100. If the IF is 455kHz, calculate: **10**
      1) The image frequency and its rejection ratio for tuning at 100kHz
      2) The image frequency and its rejection ratio for tuning at 25MHz.
   (b) Explain TRF receiver with block diagram also explain TRF sensitivity and TRF selectivity characteristics. **10**

4. (a) Explain the process of quantization in PCM. Determine the signal to noise ratio at the output. **10**
   (b) "In PCM, SNR can be controlled by transmission bandwidth" Justify. Compare PCM and Delta modulation. **10**

5. (a) Explain the ratio detector with the help of circuit diagram and explain its merits. **10**
   (b) Explain PAM, PWM, PPM generation and detection. **10**

6. (a) Compare digital signal and analog signal transmission. **5**
   (b) Derive Friis formulas for noise. **5**
   (c) Explain the slope overload and granular noise in Delta modulation. **5**
   (d) Explain FDM with neat block diagram **5**

SE Sem IV CBSGS Electronics EM 10/6/16

Q.P. Code : 548300

(3 Hours) **[Total Marks : 60**

N.B. : (1) Question No. **1** is **compulsory**
(2) Figures to the right indicate **full** marks
(3) Solve any **three** questions out of remaining **five** questions
(4) Assume suitable data if necessary

1. Solve any **three**
   (a) Define the slip of an induction motor. Explain its significance. **5**
   (b) Explain the construction of permanent magnet synchronous motor. **5**
   (c) Draw and explain block diagram V/f control using converter-inverter scheme for 3 phase induction motor. **5**
   (d) Explain back emf equation of a dc motor. **5**

2. (a) Explain the principle of operation of capacitor start and capacitor run single phase induction motor along with slip-torque characteristics and applications. **7**
   (b) Explain construction and working of multistack variable reluctance stepper motor. **8**

3. (a) A 4 pole 3 phase 50Hz star connected induction motor has full load slip of 6% calculate full load speed of the motor. **7**
   (b) Explain double field revolving theory in single phase induction motor. **8**

4. (a) Classify the brushless DC motor and explain in detail unipolar brushless Dc motor **7**
   (b) A 800W, 115V, 60Hz capacitor start motor draws 13.8 A from the supply at rated load if the efficiency is 70% and rated speed is 1800 rpm. Calculate **8**
      (i) Input power at rated load
      (ii) Power factor at rated load
      (iii) Rated motor horse power

5. (a) Explain different speed control methods of DC short motor. 7
   (b) Explain construction and working of 3 phase squirrel cage induction motor 8

6. Write short notes on
   (a) Advantages of brushles DC motor. 5
   (b) Three point starter of DC shunt motor. 5
   (c) Starting methods of 3 phase induction motor 5

SE/ Elex/Sem IV/ old/ Advanced Engg. Maths

13/05/2016

Q.P. Code : 546801

(3 Hours) **[Total Marks : 100**

OLD COURSE

Note : - 1) Question number 1 is compulsory.

2) Attempt any four questions from the remaining six questions.

3) Figures to the right indicate full marks.

Q. 1 . a) Find the eigen values and eigen vectors for $A = \begin{bmatrix} -1 & 4 \\ 2 & 1 \end{bmatrix}$ 5

b) The probability distribution function of random variable is $f(x) = k(x - x^2)$ $in\ 0 < x < 1$

find k, mean and variance. 5

c) Find the residues of $f(x) = \frac{z+1}{(z+4)(z-1)^2}$ 5

d) IF $f(x) = 3x^2 + 1$ wrere f: R →R .Check whether f is surjective function. 5

Q.2 . a) Evaluate $\int_c \frac{z-1}{z^2-4} dz$ where C is i) $|z - 2|=1$ ii) $|z + 2| = 1$ iii) $|z| = 0.5$. 6

b) If $A = \begin{bmatrix} \frac{\pi}{2} & \pi \\ 0 & \frac{3\pi}{2} \end{bmatrix}$ Find cosA. 6

c) Show that $A= \begin{bmatrix} 8 & -8 & -2 \\ 4 & -3 & -2 \\ 3 & -4 & 1 \end{bmatrix}$ is diagonable .Find the diagonal matrix and the

diagonalising matrix. 8

Q. 3. a) Fit the poisson distribution for the following data 6

x	0	1	2	3	4	5
f	142	156	69	27	5	1

b) If $A=\begin{bmatrix} 1 & 0 \\ 0 & 2 \end{bmatrix}$ Find e^A 6

c) Evaluat $\int_0^{2\pi} \frac{d\theta}{13+5sin\theta}$. 8

[TURN OVER

Q. 4 . a)In a normal distribution 31% items are under 45 and 8% are over 64 . Find the mean standard deviation. 6

b) If $f(x) = 2x^2+3$ and $g(x) = 4x+3$ .Test whether the inverse function for both f and g exist.

Also find fog and gof 6

c) Find all possible expansions if $f(z) = \frac{z+1}{z^2+5z+6}$ about z=0 indicating the region of convergence. 8

Q. 5. a) Varify Caley Hamiltons theorem and find A^{-1} for A = $\begin{bmatrix} 5 & -6 & -6 \\ -1 & 4 & 2 \\ 3 & -6 & -4 \end{bmatrix}$ 6

b) Find the mean and varience for binomial distribution. 6

c) Check whether A = { 2,4,12,16} and B = {3,4,12,24} are lattices under divisibility .also draw the Hasse Diagram . 8

Q 6 . a)A random variable X has mean 5 and varience 5 and Y has mean -2 and varience 3 . Find

i) E(2X+3Y) , V(2X+3Y) ii) E(3X-4Y+5) , V(3X-4Y+5) 6

b) Show that A = {0,1,2,3,4,5} is a finite abelian group under addition modulo 6. 6

c) A certain drug administered to 12 patients resulting in the following changes in their blood pressure

5,2,8,-1,3,0,6,-2,1,5,0,4

Can we conclude that the drug increases the blood pressure? 8

Q.7. a) Is $(Z_6 \ + *)$ an integral domain? Is it Field? 6

b) Show that $A=\begin{bmatrix} 5 & -6 & -6 \\ -1 & 4 & 2 \\ 3 & -6 & -4 \end{bmatrix}$ is derogatory. 6

c) Can it be concluded that the average life span of an Indian is more than 70 yrs if a random sample of 100 indians has an average life span of 71.8yrs with standard deviation of 7.8 yrs. 8

TE|SEM V|EIEX|CBSGS|DLIC

Extra

17/05/2016

QP Code : 31088

(3 Hours) **[Total Marks : 80**

N. B. : (1) Question No. 1 is **compulsory.**
(2) Solve any **three** out of remaining questons.
(3) Assume suitable data if necessary.

1. (a) Explain behaviour of op-amp in linear and saturation region with neat graphs. **20**
   (b) Explain non-inverting comparator with suitable example.
   (c) State various methods to achieve analog to digital conversion.
   (d) Explain 78XX series voltage regulator.
   (e) Implement y = 3 va – 5 vb + 7 vc using op-amp, where y is output and va, vb & vc are inputs.

2. (a) Derive expression for voltage gain of inverting amplifier and hence design the same for voltage gain = 20. **10**
   (b) Design a 2nd order KRC low pass filter with a cutoff frequency fo = 1 KHz and Q = 5. **10**

3. (a) Draw the circuit diagram of an inverting type schmitt trigger circuit. Design such a circuit to meet UTP = + 2.5 V & LTP = – 1 V Assume ± vsat = ± 12 V, for an input of 8sinwt, plot the graph of vo and vin. **10**
   (b) Explain working of Wien bridge oscillator and hence design for fo = 5 KHz. **10**

4. (a) Explain R/2R ladder type DAC **10**
   (b) Design Mono stable multivibrator using IC 555 to generate output delay of 10 msec. **10**

5. (a) Design voltage regulator using IC 723 for Vo = 10 V and I_L = 200 mA. **10**
   (b) Explain internal diagram of power amplifier LM 380 **10**

6. Write short notes on :– **20**
   (a) Sample and Hold circuit
   (b) V-I converter
   (c) Applications of IC 555
   (d) Switching mode voltage regulator

FW-Con. 10269-16.

TE/Sem V/ E/Ex/ CBSGS/ MCA

23/05/2016

QP Code : 31131

(3 Hours) Total Marks: 80

N.B. 1) Question **number 1** is compulsory.
2) Attempt **any three** from remaining five questions.
3) Assume suitable data wherever necessary.
4) Figure to **the right** indicates full marks.

Q1. Attempt any four from the following. (20)

a) Explain the difference between RET and RETI instructions as implemented in 8051 architecture.
b) What is the maximum address range of conditional jump instructions for 8051 architecture and justify the reason for the same.
c) Illustrate the circuit representation for interfacing single LED and relay to the port pins of 8051 architecture based processor.
d) Explain pipelining feature in ARM7TDMI architecture. Justify advantages and disadvantages.
e) Explain the significance of letters and numbers in – 'ARM7TDMI'.
f) Explain the bit orientations of CPSR register for ARM7TDMI architecture.

Q2a) Write a note on the various modes of operation of ARM7TDMI based processor. (10)

b) Explain the following 8051 architecture based instructions:
a) MOV C,0X10 b) MUL AB c) MOVC A, A+@0x2000 d) INC 0X45
e) ANL A,@R0 (10)

Q3 a) With a neat circuit representation illustrate interfacing of a typical 8-bit DAC to 8051 architecture based processor. Using DAC write a program in 8051 assembly to generate a triangular wave. (12)

b) Explain the programmer's model (register structure) in ARM7TDMI architecture. (08)

Q4a) Explain the various addressing modes with suitable examples available in 8051-architecture. (10)

b) Using internal timers write a program in 8051 assembly to generate a square wave of 10kHz frequency and 50% duty cycle on port pin P1.0. (10)

[TURN OVER

Q5)a) Explain the following ARM7TDMI architecture based instructions as well as their implications. (10)

a) BL Square b) ADD R0, R1, R2, LSL#3 c) MOVEQS R1,R0 d) LDR R8, [R3, #4] e) STR R2, [R1, #0x100]

b) Write a brief note on the process of interrupts and their mechanism of acknowledgement in 8051 – architecture. (10)

Q6) Write brief notes on.

a) ARM7TDMI thumb mode of operation. (07)

b) Interfacing stepper/continuous motor to 8051 based microcontroller. (07)

c) Serial port and modes of operation in 8051 architecture. (06)

TE/Sem V/CBSGS/Elex/SS

27/05/2016

Q.P. Code : 31172

(3 Hours) **[Total Marks : 80**

N.B.: (1) Question **No.1** is **compulsory**.
(2) Attempt **any Three** out of remaining **Five** questions.
(3) Assume suitable **data** wherever **necessary**.
(4) **Answer's** should be in **serial order**.

1. (a) Check for periodicity of the following signals. Also find the new period. **20**

(i) $x(t) = 3\cos(15\pi t) + 4\cos\left(35\pi t - \frac{\pi}{4}\right) + 8\sin(55\pi t)$

(ii) $x(n) = 3\cos^2\left(\frac{\pi}{6}n\right) + 2\cos^2\left(\frac{\pi}{4}n\right)$

(b) Determine whether the given signal is energy or power signal. Hence obtain its energy power accordingly.

(i) $x(t) = 4 \sin t \quad -\infty < t < \infty$

(ii) $x(n) = \left(\frac{3}{7}\right)^n u(n)$

(c) Plot $x(t) = u(t) - r(t) + r(t-1)$. Hence plot its even and odd parts also.

(d) Prove time shifting property of Z - transform.

(e) Check for Dynamicity, Linearity, Time variance, causality of the system.

(i) $y(t) = t\,x(t) + x(t-1)$

(ii) $y(n) = 3x(-n) + 4$.

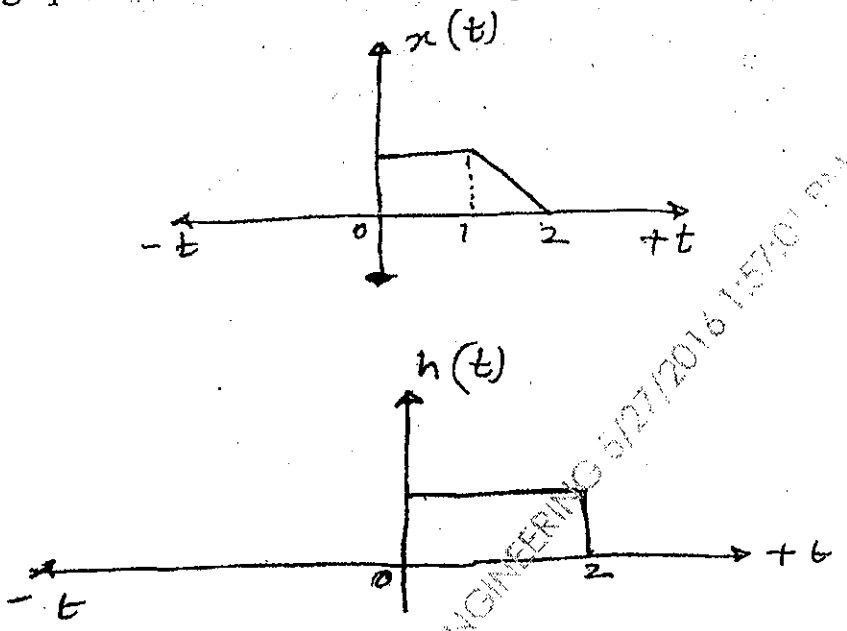
2. (a) Obtain inverse Z - transform for all possible ROC's. Also comment on Causality and Stability in each case. **10**

$$H(z) = \frac{z(3z-7)}{\left(z-\frac{1}{4}\right)(z+2)}$$

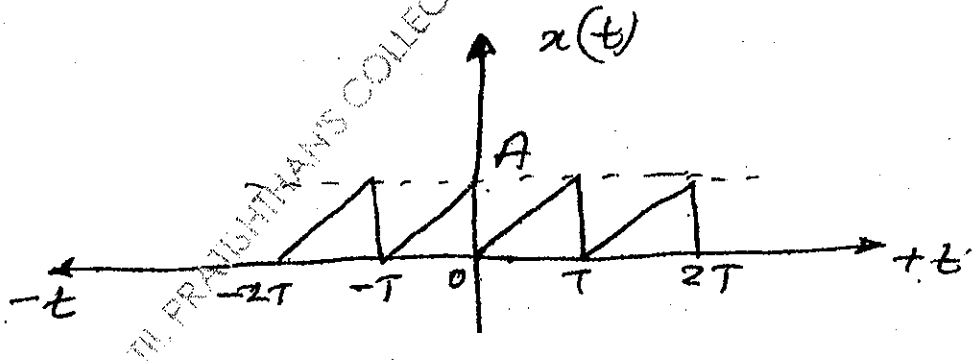
(b) State and prove Time Shifting and Convolution property of Continous Time Fourier Transform. **10**

TURN OVER

3. (a) Obtain graphical convolution of following two signals. 10



(b) Obtain exponential Fourier series of the following signal. 10



4. (a) Determine h(t) for all possible ROC's. 10

If T. F. $= H(s) = \dfrac{2s+7}{(s+2)(s-3)}$

Also comment on Causality and Stability of the system for each case.

(b) A causal DT LTI system is described as 10

$$y(n) = 3y(n-2) + 4y(n-1) + x(n)$$

Obtain : (1) T.F. of system

(2) Obtain step response

(3) Obtain response if input $x(n) = \left(\frac{1}{2}\right)^n u(n)$

(4) Also plot pole's and zeros of the T.F. and comment on causality and stability.

10

5. (a) Determine Impulse response and step response of a CT LTI system.

$$\frac{d^2y(t)}{dt^2} + \frac{7dy(t)}{dt} + 12y(t) = x(t)$$ 10

(b) Obtain auto-correlation of following signals

(i) $x(t) = 3e^{-2t}\ u(t)$

(ii) $x(n) = \left(\frac{3}{4}\right)^n u(n)$

10

6. (a) Obtain DT Fourier Transform of following signal $h(n) = [2\ 1\ 2]$ plot its magnitude and phase spectrum. 10

(b) Obtain :

(i) Z - transform of

$$x(n) = n\left(\frac{3}{4}\right)^n u(n) + u(n-1)$$

(ii) Laplace transform of

$$x(t) = t.e^{-3t}\ u(t) + t\ u(t-1)$$

Use properties of transform only.

TE Sem V CBSGS Elex Digital Commn 2/6/16

QP Code: 31216

(03 hours) [Total marks : 80

N.B. : 1) Question no. 1 is compulsory
2) Attempt **any three** questions out of the remaining five questions
3) Assume suitable data if required, stating them clearly.

Q. 1 **Answer the following questions: (any four)** (20)

(a) What is a random variable? Explain the moments of a random variable viz. Mean and Variance.

(b) Why is MSK signal called as "shaped QPSK" signal? Justify with expressions and Waveforms.

(c) Discuss source coding and channel coding in brief with example.

(d) The binary data 1101101101 is applied to the input of duo-binary system with a pre- coder. Construct duo-binary coder with the corresponding output.

(e) State and explain Shannon-Hartley theorem.

Q 2 (a) Show that for an input signal which is a sequence of rectangular positive and negative pulses, the integrator is the matched filter. Bring out properties of matched filter. (10)

(b) With the help of neat block diagram and waveform, explain how a message is transmitted in BFSK? What type of receiver is used for BFSK reception? Explain its working. (10)

Q.3 (a) A discrete memory less source has an alphabet of five symbols with the probabilities-

Symbol	S1	S2	S3	S4	S5
Probability	0.30	0.20	0.16	0.10	0.15

(i) Construct Huffman code , find entropy and average length of the code.

(ii) Calculate code efficiency and the redundancy of the code. (8)

(b) For K=3 , code rate=1/3 , of a Convolution Code encoder with generator Vectors given as g1=[101], g2=[110] and g3=[111] , draw the encoder diagram.
(i) draw its State diagram and Code tree.
(ii) Use the Code tree to find the codeword for the msg 1011. (12)

P.T.O

FW-Con.11957-16.

Q.4 (a) With reference to 8-PSK, explain the following:
(i) transmitter and receiver with a neat block diagram along with mathematical expression for transmitted signal
(ii) sketch its PSD indicating the bandwidth
(iii) draw its constellation diagram and find its Euclidian distance (5+3+2)

(b) Design a Feedbck shift register encoder for a (8,4) cyclic code with generator Polynomial $g(x) = (1+x+x^2+x^3)$.
(i) Find the codeword for the msg 1001, By tracing the path through the encoder.
(ii) draw the syndrome calucalator for the same and find the syndrome if the received codeword is 1101110 (5 +5)

Q.5 (a) What is ISI ? How is it caused? Discuss the remedies to overcome ISI. state the Nyquist's Condition for zero ISI (Distortion less transmission) (10)

(b) Explain Direct sequence spread spectrum system.and Define anti-jamming characteristics of spread spectrum system.

If the direct sequence spread spectrum system has the following parameters.:

Data sequence bit duration Tb=6.125 ms

PN chip duration Tc=1.5 microseconds

The probability of error is less than 10^{-5} (Eb/No=10)

Then calculate Processing gain and Jamming margin. (5+5)

Q.6 (a) Draw the signal constellation diagram for 16-ary QASK (with d=2a) and for 16-PSK System. determine the Euclidian distance for the both systems and Compare. Which of them has better noise immunity? (10)

(b) write short notes on : any two (10)

(i) Central Limit theorem

(ii) Shannon-Fano coding with an example

(iii) comparison of Offset QPSK and non-offset QPSK

(iv) Linear Transversal Equalizer

E1ex/TE/SEMVI/BVD/CBSGS/10/5/16

Q.P. Code : 591600

(3 Hours) **[Total Marks :80**

N.B. : (1) **Question** No.1 is compulsory.
(2) Attempt any **three** out of remaining.
(3) Assume suitable data wherever required.

1. (a) Draw and explain AND gate using pass transistor logic. **20**
(b) Explain drawhack of dynamic CMOS design.
(c) Draw and explain manchester carry circuit.
(d) What are various programming techniques used for EEPROM in Explain them in short.

2. (a) Draw 6T SRAM cell and explain it's read and write operation. **10**
(b) Define scaling ? Explain various types of scaling in detail. **10**

3. (a) Explain latch up condition in CMOS in detail. What are remedies to avoid latchup. **10**
(b) Give and explain the drawback of ripple carry adder. Explain 4 bit CLA adder with it's carry equations, logical network using dynamic CMOS logic. **10**

4. (a) Explain how ESD (electrostatic discharge) affect the MOSFET. Give and explain input protection circuits. **10**
(b) Give and explain interconnect scaling with its width, length, thickness and capacitances. **10**

5. (a) Explain various technique of clock generation. Discuss 'H' tree clock distribution. **10**
(b) Consider a CMOS inverter circuits with following parameters **10**

VDD = 3.3v VTon = 0.6v VTop = - 0.7v, $\mu_n C_{ox}$ = 60 μ A/v², $\left(\frac{W}{L}\right)_n$ = 8

$\mu_p C_{ox}$ = 20 μA/V², $\left(\frac{W}{L}\right)_p$ = 12. Calculate the noise margin.

6. Write a short note on **20**
(1) Sense ampliter
(2) Barrel shifter
(3) Interconnect parameters

Con.8159-16.

TE/SEM VI/ Elex/ CBSGS/ AIS

16/05/2016

QP Code : 591702

(3 Hours) **[Total Marks : 80**

N.B. (1) Question No.1 is **compulsory.**
(2) Attempt any three questions from remaining five quesitons.
(3) Assume suitable data if necessary.
(4) Figures to the right indicate full marks.

1. (a) With neat block diagram, explain the working of multichannel data acquisition system. **10**
   (b) Why converters are required? Explain electrical to pneumatic converter. **10**

2. (a) Draw and explain single and double acting actuators. **10**
   (b) Explain the installation procedure of control valve. **10**

3. (a) Explain the working of smart transmitters. Highlight the features of smart transmitter. **10**
   (b) With neat diagram, explain the cascade of PID controller. **10**

4. (a) Compare electrical, pneumatic and hydraulic actuators. **10**
   (b) Draw and explain inherent and installed characteristics of control valves. **10**

5. (a) With neat diagram, explain the instrument air system. **10**
   (b) Explain the working of electronic DP transmitter. **10**

6. (a) Explain process reaction curve method and ZN method of PID tuning. **10**
   (b) With neat diagram, explain speed control circuit for hydraulic actuator. **10**

TE|SEMVI/CBSGS|EIEX|CO 20|5|16

Q.P. Code : 591801

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question **No.1** is **compulsory.**
(2) Attempt **any Three** questions from remaining **questions.**
(3) **All** questions carry **equal marks.**
(4) **Figures** to the **right** indicate **full marks.**

1. (a) Explain single and double precision format for floating point number representation. **5**
   (b) Write in brief on nano-programming. **5**
   (c) Draw Register structure of IA-32 family. **5**
   (d) Explain SIMD computer organization. **5**

2. (a) Explain performance measure of computer architecture and factors to improve the performance of the system. **10**
   (b) What is microprogramming ? Draw and explain Micro programmed control unit. **10**

3. (a) Explain sequence counter method of implementing Hardware control unit. **10**
   (b) What is LRU Algorithm? Find the page fault for the following string using FIFO and LRU page replacement policies for the page address stream 6 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 5. Consider page frame size n = 3. **10**

4. (a) What are the different cache mapping techniques? **10**
   Consider a cache consisting of 128 blocks of 16 words each, for a total of 2048 (2k) words and assume that the main memory is addressable by a 16 bit address and it consists of 4k blocks. How many bits are there in each of the TAG, BLOCK/SET and WORD fields for different mapping techniques.
   (b) Explain in brief about various DMA transfer modes. **10**

5. (a) Explain Address translation with respect to virtual memory. Hence explain use of Translation Look aside Buffer (TLB). **10**
   (b) Compare RISC and CISC architectures. **5**
   (c) Write a note on addressing modes of IA- 32 family. **5**

6. (a) Explain data hazard and code hazard in pipelining. Mention solutions to minimize the hazards. **10**
   (b) What is bus contention? How is it resolved by using bus arbitration? Explain various bus arbitration methods. **10**

TE/Sem VI/CBSGS/PE-I/ELEX 26/5/2016

QP Code :591902

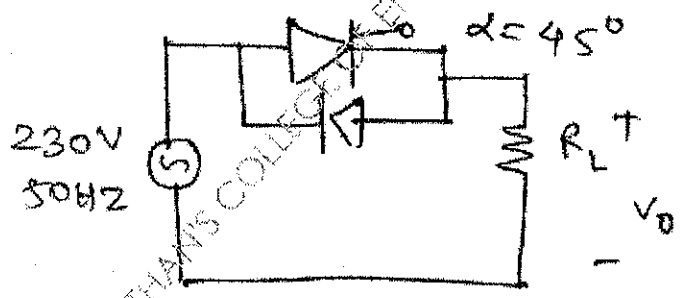
(3 Hours) [Total Marks :80

N.B. : (1) **Question** No. 1 is **compulsory**.
(2) Attempt any **three** questions out of remaining **five** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) Draw and explain dynamic turn on characteristics of SCR **5**
(b) What is the need of commutation. Explain the any one method of forced communication. **5**
(c) Define and explain performance parameters of controlled rectifier **5**
(d) Draw and explain boost converter. Derive the relation for output load voltage. **5**

2. (a) Draw and explain semi-converter with the help of circuit diagram and waveforms. **10**
(b) Draw and explain Buck-Boost converter with the help of circuit diagram and waveforms Derive the relation for load voltage. **10**

3. (a) Explain the working of three phase bridge inverter in 120^0 conduction mode with resistive load. Draw waveforms. **5**
(b) Draw the load voltage waveform for the circuit given below. **5**



(c) draw and explain SOA of power MOSFET. **5**

4. (a) A single phase semi converter is operated from 230V, 50Hz ac supply. The load resistance is 20Ω. The average output voltage is 30% of the max. Possible average output voltage. Determine **10**
(i) Firing angle
(ii) RMS and Average output current
(iii) RMS and average thyristor current
(b) Explain in brief single phase cyclo-converter with circuit diagram and waveforms. **5**

[Turn Over

(c) Explain the need of neutrilisation of harmonics of inverters. **5**

5. (a) Explain the working of AC full wave control circuit using DIAC-TRIAC. **10**
Draw waveforms across load and TRFAC for $\alpha = 60^0$. Derive relation for RMS load voltage.

(b) Explain the multiple pulse width modulation in inverters. Explain the neutrilisation of harmonics. **10**

6. (a) Single phase full bridge inverter has a resisistive load of R = 3Ω and the dc input voltage Edc = 50V. compute **10**
   (i) The average output power Po
   (ii) The average and peak current of each thyristor.

(b) Draw and explain switching cha. of GTO **5**

(c) Draw and explain snubber circuit. **5**

TE sem VI CBSGS Electronics MITM 07/06/16

Q. P. Code : 592100

(2 Hours) **Total Marks-40**

Note:

i. Q.1 is compulsory
ii. Attempt any three questions from remaining five.
iii. Each question carries **10** marks.

1. Answer any five.

a. Write any four top security concerns. **2**
b. Define OSI layers. **2**
c. Write a small note on E-business. **2**
d. What is search engine? **2**
e. Explain network management. **2**
f. What is data mining? **2**
g. Which are the components of IT Infra? **2**

2.

a. Define topology. Explain any three common topologies. **5**
b. Define cabling. Classify cable types and explain in detail. **5**

3.

a. Explain open source software with examples. **5**
b. Write a detailed note on firewall. **5**

4.

a. Explain the benefits of intranet. **5**
b. State the types of network. How is optical network different from wired network? **5**

5.

a. Discuss the TCP/IP stack. Also list the various functions of the internet protocol. **5**
b. Explain the following terms related to storage. **5**
i) Online storage
ii) Near line storage
iii) Offline storage

6. Write a note on following terms related to IT audit. **10**
i) Information audit.
ii) Audit schedule
iii) Audit plan
iv) Audit preparation
v) Internal audit.

BE/ Elex/ Sem VII/ ESD
(CBSGS)

13/05/2016

QP Code : 31253

(3 Hours) Total Marks: 80

N.B. 1) Question number 1 is compulsory.
2) Attempt any three from remaining five questions.
3) Assume suitable data wherever necessary.
4) Figure to the right indicates full marks.

Q1. Attempt any four from the following (20)
a) Describe design metric and optimization challenges for embedded system
b) Explain serial peripheral interface. Compare it with parallel method
c) Explain some features of cortex R and A series which are not available in M series
d) What is on chip debugging feature? How it is accessed?

Q2a) What are communication means available for networking industrial field devices? (10)
b) What architectural features of cortex-M3 make it low power device. (10)

Q3a) Describe any two wireless communication means used for embedded system. (10)
b) Describe any three RTOS scheduling methods and compare. (10)

Q4 Design a driver-less car system. Show hardware block diagram, system working model (FSM), software architecture module/function/drivers and their relationship, list of components. (20)

Q5a) Which features of c-programing may be specifically useful in embedded system? How? (10)

b) Interface any sensor/display device with any controller. (10)

Q6 Write short notes on, (20)
a) Digital design using Verilog/vhdl: Advantages/Disadvantages
b) MSP430 architecture compared against Cortex-M3 based architecture
c) Prominent features of Cortex M3 and its impact on design, development and maintenance

BE/EXTC/sem VII/CBSGS/IC Technology QP Code : 31293 19/5/16

Extra

Time: 3 Hours. Max. Marks: 80

EXTRA

N.B.

1) Question No. 1 is compulsory
2) Solve any three questions from the remaining questions
3) Assume suitable data if necessary

1. Solve any four of the following (20)
   (a) Explain Interstitial and substitutional diffusion process.
   (b) Explain Electronics package reliability.
   (c) Explain the concept of clean rooms.
   (d) Explain Nuclear and electronic stopping mechanisms in Ion implantation with neat diagrams
   (e) Give the steps in a standard RCA cycle during wafer cleaning

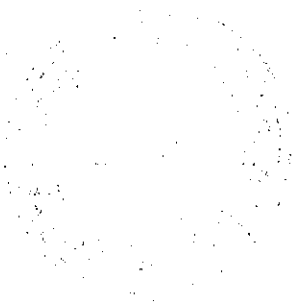
2.
   (a) What is Ion implantation? Explain the process with a neat diagram. (10)
   (b) Describe optical lithography with the help of a neat diagram. (10)

3.
   (a) Explain the fabrication process step along with vertical cross-sectional views for CMOS inverter using twin tub process. (10)
   (b) With neat diagram explain the Float Zone technique of crystal growth. (10)

4.
   (a) What is the significance of Design rules? Draw layout for the CMOS inverter using lambda (λ) based design rules. (10)
   (b) Discuss Etching methods for photoresists removal. (10)

5.
   (a) Explain SOI fabrication using bonded SOI and smart cut method. (05)
   (b) State advantages of BICMOS over CMOS (05)
   (c) Describe with the help of a neat diagram Hayness-Schokley experiment for measurement of Drift Mobility of n-type semiconductor. (10)

6. Write short notes on any four of the following (20)
   (a) MODFET and optoelectronics devices
   (b) Nanowire transistor
   (c) Molecular Beam epitaxy
   (d) Second order effects in bipolar transistor
   (e) VLSI Technology Trends affecting Testing



BE| Sem VII| E&C| CBSGS| Power Electronics - II

25/05/2016

Q.P.Code **31331**

(3 Hours) [Total Marks : 80

N.B. : 1. Question **No.1** is compulsory.
2. Solve any **three** questions out of remaining five questions .
3. Assume suitable data if necessary .

Q1 Attempt any **four** from the following : **20**

a) Why separately excited DC motor is widely used as compared to DC shunt motor ? Explain

b) Give advantages of regenerative braking of DC motor compared to other methods of braking ?

c) Explain why V/F control is popular in AC induction motor control.

d) Give advantages of high frequency induction heating as compared to convertional methods of heating.

e) Compare SMPS with linear regulated power supply.

Q2 a) Explain the effect of soruce inductacne in single-phase full converter working in rectifier mode. Draw relevant output voltage waveforms Give equations which can be used to determine overlap angle μ and output DC voltage. **10**

b) In a 3-phase full converter working in rectifier mode, input supply is 440V (L-L), 50Hz. If firing angle $\alpha = \pi/4$ and load current is 20 A constant with load voltage = 370 V, determine source inductance Ls and overlap angle μ. **10**

Q3 a) Explain the steps involved in space vector modulation (SVM) technique used in three-phase voltage source inverter. **10**

b) Explain using block diagram and transfer funtion, working of PI controller for DC-DC converter . **10**

Q4 a) Give details of the state-space averaged model of DC-DC buck converter operating in continous conduction mode. **10**

b) A separately excited DC motor armature winding is supplied power using single-phase full bridge converter working on 250V, 50Hz mains supply. If Ra = 0.1 Ω and armature urrent is 50 A, find the firing angle of the converter at 700RPM. Assume that field winding is supplied with rated DC voltage and motor ratings are 110V DC,1000 RPM and 75A. **10**

Q5 a) Explain rotor resistance method of speed control of three-phase wound rotor induction motor. Draw speed-torque characteristics and give disadvantages of this technique. **10**

[TURN OVER

b) Explain the following regions as related to V/F control of AC induction motor. 10
   i) Contant torque
   ii) Contant power
Draw variations in applied voltage and motor current over entire operation from low speed to double the rated speed of the motor.

Q6 Write short notes on :
a) Battery charging circuit and its working 7
b) Selection of battery capacity in UPS. 7
c) Constant torque and constant power regions in control of separately excited DC motor. 6

Extra

BE/Sem VII/Old/Elex/PED

25/05/2016

QP Code : 29832

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question **No. 1** is **compulsory.**
(2) Solve **any four** questions out of remaining **six** questions.
(2) **Figures** to the **right** indicate **full** marks.

1. (a) What do you understand by subsynchronous speed and super-synchronous speed of Ac motor. **5**
   (b) Differntiate between voltage source invester and current source invester. **5**
   (c) Explain class A chopper and derive the relation for o/p voltage. **5**
   (d) Explain the need of harmonic reduction in inverter. **5**

2. (a) What do you understand by dual converter. Explain it with the help of circuit diagram and waveforms. **5**
   (b) Explain multiple PWM to control the output voltage in investers. How it reduces harmonics present in the o/p. **5**

3. (a) Draw and explain voltage commutated chopper with the help of waveforms. **10**
   (b) Draw and explain off-line ups and on-line ups. State advantages and dis-advantages of each type. **10**

4. (a) Explain Basic series invester wish the help of circuit diagram and wave forms. **10**
   (b) With the help of block schematic explain v/f control scheme to control the speed of three phase induction motor. **10**

5. (a) For a current commutated chopper, peak commutating current is thrice the maximum possible load current. The source voltage is 220V dc and main SCR turn-off time is 20μs. For a maximum load current of 180A, Compute. **10**
      (a) The value of commutating components L and C.
      (b) The maximum capacitor voltage.
      (c) The Peak commutating current.

   (b) Explain the rotor resistance control technique to control the speed of three phase induction motor. **10**

[TURN OVER

6. (a) Explain the working of flyback converter in dis contineous and contineous current mode. Draw waveforms. 10

(b) Explain the effect of source inductance in fully controlled bridge converter with R-L load. Derive the relation for load voltage and load current. 10

7. Write short notes on

(i) Class E chopper 7

(ii) Slip Power recovery scheme 7

(iii) Slip-torque curve of induction motor. 6

BE sem VII old Electronics CN 06/06/16

QP Code : 30027

(3 Hours) **[Total Marks : 100**

N.B. (1) Question **No.1 is compulsory.**

(2) Answer any **four** out of the remaining **six** questions.

(3)Figures to the right indicates marks

(4)Illustrate answers with sketches whenever required

Q.1 Answer any four

a) Explain how microwave communication work (5)

b) Explain various LAN topology (5)

c) Explain congestion control in communication network (5)

d) Compare circuit switching and packet switching. (5)

e) Describe piggy backing in brief (5)

Q.2 a) Explain UTP, STP, coaxial cable and fibre optic cable. Also give their applications, limitations and general properties. (10)

b) Explain XDSL technology in detail. (10)

Q.3 a) Explain various frame types in HDLC. (10)

b) Explain in detail OSI model (10)

Q.4 a) Draw the block diagram of SONET and explain its operation also. Explain SONET frames (10)

b) Explain in detail any one routing algorithm (10)

Q.5 a) Explain CSMA/CD in detail. (10)

b) Explain datagram and packet switching (10)

Q.6 a) Write a note on Congestion control in Packet switching network (10)

b) Explain leased line concept and ISDN technology (10)

Que.7 a) Explain the following network connecting devices (10)

I) switches II) routers III) gateway IV) hub V) bridge

b) Explain flow control and framing in communication network (10)

—— X ——

GE-Con. 12148-16.

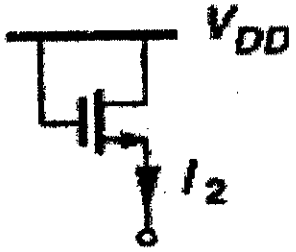
BE/Elex/Sem VIII/CMOS/CBSGS 12/05/2016

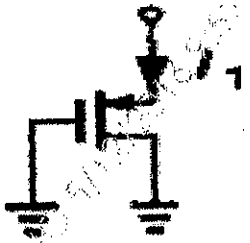
Q.P. Code : 719702

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question **ONE** is **compulsory.**
(2) Solve **any THREE** out of remaining **questions.**
(3) Draw **neat** and **clean diagrams.**
(4) Assume **suitable data** if **required.**

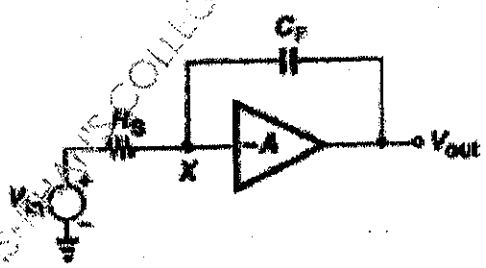
1. (a) Will the following circuits work as current sources? Give the correct reason for your answer. **5**





(b) List down the performance parameters of VCO and explain trade off between them. **5**

(c) Calculate the pole associated with the node X shown in the following figure. Assume $R_s = 1K\Omega$, $C_F = 0.1pF$ and A = 10. **5**



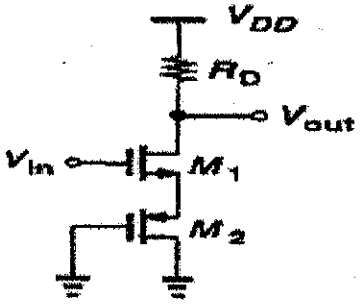
(d) Draw and explain the floor plan for a possible mixed signal chip. **5**

2. (a) Show the op-amp based implementation of temperature independent bandgap reference and various issues involved thereof. **10**

(b) For common source stage with diode connected load, if the variation of $\eta = (g_{mb}/g_m)$ with the output voltage is neglected then prove that the gain is independent of bias currents and voltages. **5**

TURN OVER

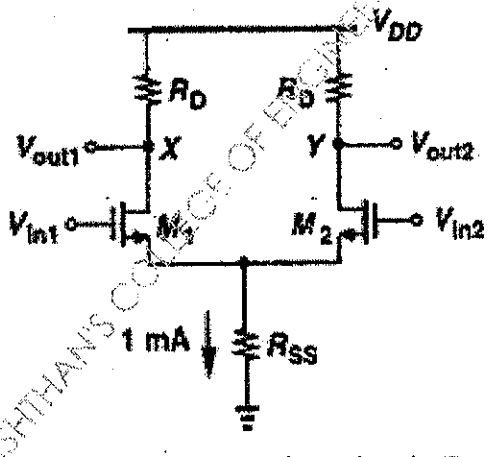
(c) Assuming $\lambda = \gamma = 0$, calculate the small signal gain of the circuit shown: 5



3. (a) The following circuit shown in Figure uses a resistor rather than a current source to define a tail current of 1mA. Assume $(W/L)_{1,2} = 25/0.5$, $\mu_n C_{ox} = 50\ \mu A/V^2$, $V_{TH} = 0.6$ V, $\lambda = \gamma = 0$ and $V_{DD} = 3$V. 10

(a) What is the required input CM for which Rss sustains 0.5V?

(b) Calculate R_D for a differential gain of 5.



(b) Explain the concept of switched capacitor circuit. Draw and explain discrete time integrator along with the output waveform. 10

4. (a) With the use of small signal behaviour, prove that for differential pair the magnitude of differential gain is equal to $g_m R_D$ regardless of how the inputs are applied. 10

(b) What is the need of compensating operational amplifiers? Explain the compensation of two stage operational amplifiers? 5

(c) Derive an expression for the input referred noise voltage of common source stage. 5

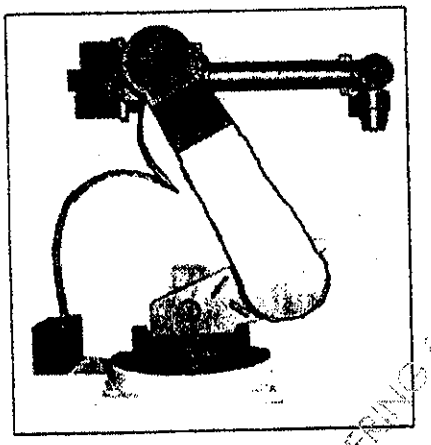
BE| SEMVIII | CBSGS| Elex| Robotics QP CODE : 732400 18|5|16

(3 Hours) [Total Marks: 80]

N. B.: 1. Question No. 1 is compulsory.
2. Attempt any three questions from the remaining five questions.
3. Assume suitable data if necessary.
4. Figures to the right indicate full marks.

Q.1. Answer following questions in brief.

a Draw the approximate workspace for the following robot. Assume the dimensions of the base and other parts of the structure of the robot are as shown below. (05)



b A point $P(7,3,1)^T$ is attached to the frame F and is subjected to following transformations. Find the coordinates of the point relative to reference frame at the conclusion of transformations. (05)

i Rotation of 90^0 about the z-axis

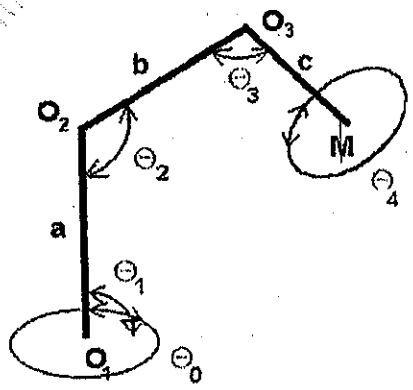
ii Followed by a rotation of 90^0 about y-axis

iii Followed by a translation of [4,-3,7]

c What is potential function? How it is used for navigation of robot? (05)

d What is thresholding? Explain with suitable example. (05)

Q.2. a A 3-DOF robot arm has been designed for applying paint on flat walls, as shown below. (15)



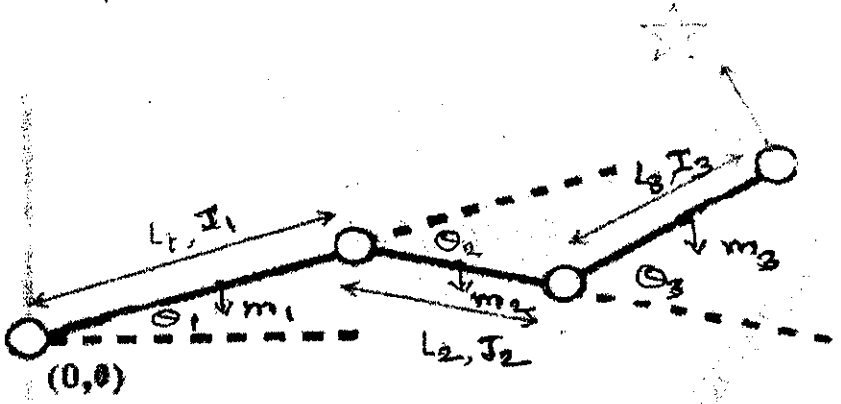
- Assign coordinate frame as necessary based on the D-H representation.
- Write parameter table.

[TURN OVER

- Write all A matrices.
- Find the ${}^{U}T_{H}$ matrix.

b Define the following terms (05)
- Euler angles
- Articulated joints

Q.3. a Derive the equations of motion for the system shown below: (08)



b A camera is attached to the hand frame T_H of a robot as given. The corresponding inverse Jacobian of the robot at this location is also given. The robot makes a differential motion described as D = [0.05 0 -0.1 0 0.1 0.03]^T. (12)

i Find which joints must make a differential motion, and by how much, in order to create the indicated differential motion

ii Find the change in the Hand frame

iii Find the new location of the camera after the differential motion

iv Find how much the differential motion should have been instead, if measured relative to Frame T_H, to move the robot to the same location as in part (iii)

$$T_H = \begin{bmatrix} 0 & 1 & 0 & 3 \\ 1 & 0 & 0 & 2 \\ 0 & 0 & -1 & 8 \\ 0 & 0 & 0 & 1 \end{bmatrix} \qquad J^{-1} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 2 & 0 & -1 & 0 & 0 & 0 \\ 0 & -0.2 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

Q.4. a Explain Tangent Bug algorithm and compare it with Bug2 algorithm. (10)

b Explain Brushfire algorithm. Discuss local minima problem. (10)

Q.5. a What is GVD? Explain sensor-based construction of GVD. (10)

b Explain how you will generate Cartesian-space trajectories. Give simple example. (10)

Q.6. Write short notes on

a Forward and Inverse kinematics (05)

b Langragian Mechanics (05)

c Visibility graph construction (05)

d Wave-front planner (05)

BE/SEM VIII/CBSGS/ EleX/MC 18/5/16

QP Code : 728300

(3 Hours) **[Total Marks :80**

N.B. : (1) Question No. **1** is **compulsory.**
(2) Attempt **any three** questions out of the remaining **five** questions.

1. Answer the following:- **20**
   (a) Explain the soft, softer and soft-softer handoff.
   (b) Explain umbrella cell approach in cellular system
   (c) Explain the services and features of GSM.
   (d) Discuss the need for 3G cellular networks.

2. (a) Explain the UMTS network architecture in detail with interfaces. **10**
   (b) Explain the CDMA 2000 technologies. **10**

3. (a) Explain the frame structure for GSM. **10**
   (b) Explain the following for GSM:
      (i) Diagonal interleaving **2**
      (ii) Ciphering **2**
      (iii) SIM **2**
      (iv) IMSI number **2**
      (v) Short Message Service (SMS) **2**

4. (a) Explain the 4G LTE architecture with a neat block diagram. **10**
   (b) Discuss Mobile IP in detail. **10**

5. (a) With a neat block diagram explain the forward traffic channel processing in COMA. **10**
   (b) Consider a cellular system in which the total available voice channels to handle traffic are 480. The area of each cell is 5sq.km and the total coverage area of the system is 3000 sq.km. **10**
      (i) For the cluster size of 7, find the no. of channels per cell, no. of clusters, and the system capacity.
      (ii) For the cluster size of 4, repeat the above calculations
      (iii) Comment on the result

6. Write short notes on any **four**: **20**
   (a) WSN
   (b) GPRS
   (c) Trunking and GOS
   (d) Mobility and resource management in CDMA
   (e) Erlang B and Erlang C system

24/5/16

BE/SEMVIII/CBSGS/Elex/MEMS Technology

Q. P. Code : 731501

3 Hours Max Marks: 80

N.B.

1) Q. No. 1 is compulsory.
2) Attempt any three out of remaining questions.
3) Assume any suitable data wherever required but justify the same.

1	a	Give few examples of MEMS device which are characterized by sensors and actuators.	20
	b	Explain the sacrificial layer and its role in fabrication of MEMS devices	
	c	What are the characteristics of Micro-heater?	
	d	In case of photolithography, Compare the two types of photo-resist used	
2	a	Discuss the process of photolithography. Mention the types of photolithography suitable for at least two MEMS devices with justification.	10
	b	Discuss selection of material based on applications. Support your answer by considering suitable example.	10
3	a	A 30 μm thick membrane is needed for a pressure sensor application. Calculate the size of the mask opening W needed for the V groove if the full wafer thickness is 600 μm using an-isotropic (Tan 54.74^0) etching below the silicon <100> surface.	10
	b	Explain Dry etching & Wet etching in fabrication process of MEMS devices.	10
4	a	Describe the representative process flow for fabricating the ink jet printer head by Hewlett-Packard. Also explain the operating principle of this MEMS device in detail.	10
	b	Differentiate between bulk and surface micromachining for fabrication of MEMS devices with suitable example	10
5	a	State various Chemical Vapor Deposition Techniques. Explain in brief the techniques of Chemical Vapor Deposition for MEMS device fabrication.	10
	b	Explain transduction pertaining to microfilm strain gauge. State the factors that lead to thin film stress	10
6		Write a short note on (any three)	20
	a	Photolithography(Compare major types of exposure system)	
	b	Anodic bonding	
	c	Reliability of MEMs devices.	
	d	Applications of MEMS in Biomedical Instrumentation	

BE/SEMVIII/REV/Elex/Robotics & Automation 24/5/16

Q.P. Code : 631202

(3 Hours) **[Total Marks : 100**

N.B.: (1) Question **No.1** is **compulsory**.
(2) Solve **any Four** from remaining **Six** questions.
(3) Assume suitable **additional data** if **necessary**.

1. (a) Explain the why Inverse kinematics solution is not unique for generic robots. **5**
   (b) What is the tool configuration vector? Explain its role in the solution of an inverse kinematic problem. **5**
   (c) Define hard/fixed, soft/flexible automation and hence the relative cost effectiveness of different types of automation with a neat sketch. **5**
   (d) Define link and joint kinematic parameters. **5**

2. (a) Find the joint position of the tool tip of the Adept One robot when the joint variables are $q = [\Pi/4, -\Pi/3, 120, \Pi/2]^T$ Where $d = [877, 0.0, d3, 200]^T$ $a = [425, 375, 0.0, 0.0]^T$. **10**
   (b) How does the SCARA arm geometry differ from the vertical articulated arm? Why is the SCARA arm more ideal for assembly applications. **10**

3. (a) Explain with diagram basic four steps for transferring Frame k-1 to frame k. **10**
   (b) Explain the inverse arm kinematics of a two DOF cylindrical coordinate robot arm. **10**

4. (a) What is the different between Path & Trajectory? Explain Trajectory planning? **10**
   (b) Explain the bounded deviation algorithm for straight line motion of the tool path. **10**

5. (a) Explain linear interpolation with parabolic blends. Discuss its advantages over piecewise linear interpolation. **10**
   (b) Explain role of line and area descriptors for analyzing shape of an object. **10**

6. (a) Explain with ladder diagram PLC system for dispensing oil from tank. **10**
   (b) What are the advantages and disadvantages of PLC system. **10**

7. Write notes on the following : **20**
   (a) Classification of robots
   (b) Template matching technique for part recognition
   (c) Link co-ordination arm equation
   (d) Robot specification

BE/ Elex/ sem VIII / CBSGS / ANT

30/05/2016

Q.P. Code : 733701

(3 Hours) **[Total Marks : 80**

N.B.: (1) Question **No. 1** is **compulsory**.
(2) Attempt **any Three** from the remaining.
(3) **Figures** to the **right** indicate **full marks**.
(4) Assume suitable **data** wherever **required**.

1. Attempt **any Four** from the following : **20**
   (a) Draw and describe ATM cell in detail.
   (b) Explain SONET frame format with neat diagram.
   (c) Describe the term DMZ.
   (d) What is the need of DWDM ? Explain its working principle.
   (e) Draw and explain different states of devices in Bluetooth.

2. (a) Describe ubiquitous and hierarchical access and compare them. **10**
   (b) With the neat diagram, explain frame format of Frame Relay, How congestion control is implemented in it. **10**

3. (a) Explain Bluetooth protocol stack. **10**
   (b) Explain ATM protocol architecture in detail. **10**

4. (a) Draw and explain IEEE 802.15.4 LR-WPAN Device architecture. **10**
   (b) With respect to network management, explain following terms : **10**
   (1) Documentation
   (2) OAM & P

5. (a) Explain network security threats and network security safeguards. **10**
   (b) What is firewall? What are the capabilities and limitation of firewall ? Discuss different types of firewall. **10**

6. Write a short note on **Any Four** : **20**
   (a) NAT
   (b) Role of VCI and VPI in ATM
   (c) SNMP
   (d) Steps for completing the Access N/W Design
   (e) Packet filtering

BE Sem VII CBSGS Electronics DIP 06/06/16

QP Code : 31535

(3 Hours) **[Total Marks : 80**

N.B. (1) Question No. 1 is compulsory.
(2) Attempt any three questions from remaining.
(3) All questions carry equal marks.
(3) Assume suitable data wherever necessary.

Q.1 Answer any Four of the following:
a) Explain the components of Image processing system. (5)
b) List properties of 2D DFT. (5)
c) Explain Erosion and Dilation in brief. (5)
d) Justify, "Huffman coding is a lossless compression technique". (5)
e) Why is the sum of coefficients of a high pass filter mask zero? (5)

Q.2 a) Define Image Enhancement. Explain the following enhancement operations and draw the graphs of transformation function: (10)
1. Bit plane slicing 2. Gray level slicing

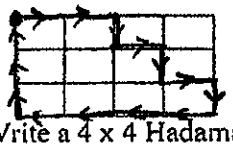
b) An 8 level image is given below. Perform Histogram equalization and draw histograms of original and equalized images. (10)

4	6	0	3	7
2	1	5	0	3
4	2	7	0	7
1	5	4	6	0
4	7	5	4	1

Q.3 a) Perform edge detection using graph theoretic technique for the image segment shown below. Assume that edge starts from first row and ends by third row. Find the edge corresponding to minimum cost path. (10)

7	5	2
1	2	4
2	4	3

b) What are chain codes? Obtain the four directional and eight directional chain codes for the boundary shown below: (10)



Q.4 a) What is Hadamard Transform ? Write a 4 x 4 Hadamard matrix and ita applications. Is H(4) ortogonal and normalized. (10)

b) Explain the following morphological operations:- (10)
i) Hit and Miss Transformations
ii) Opening and Closing

Q.5 a) Generate the Huffman code for the sentence: "COMMITTEE" (10)
Calculate entropy of the source, average length of the code generated and coding efficiency.

b) What are the different types of data redundancies present in a digital image? Explain them. (10)

Q.6 Write short notes on any three of the following:- (20)
a) JPEG
b) DWT
c) Image sampling and Quantization
d) Isopreference Curves

BE| SEM VIII| [redacted] OLD| Elex| AND 12|5|16

Q.P. Code : 630702

(3 Hours) **[Total Marks :100**

N.B. : (1) Question No. **1** is **compulsory,**
(2) Attempt any **four** out of remaining **six** questions,
(3) Assume any suitable data whenever required and justify the same.

1. (a) Draw and explain Carry save adder **5**
   (b) Design SR flipflop using AOI ,write Verilog HDL **5**
   (c) Explain electromigration effect in an interconnect. **5**
   (d) Write Verilog code for 8 bit counter. **5**

2. a) What would be the conductor width of power and ground wires to a 50 MHz clock buffer that drives 100 pF of on-chip load to satisfy the metal-migration consideration (J_{AL} = 0.5mA/μm)? What is the ground bounce with chosen conductor size? The module is 500 μm from both the power and ground pads and the supply voltage is 5 volts. The rise/fall time of clock is 1 ns. (Assume sheet resistance of wire = 0.05Ω/sq). **10**
   (b) Draw 1T DRAM cell and explain its write, read, hold and refresh operation. **10**

3. (a) Explain 4-bit CLA adder with its carry equations, logical network and writs its Veri log description. **10**
   (b) Explain in detail the input protection circuit for CMOS, also explain output circuit with I/O circuit **10**

4. (a) Give and explain the maximum and minimum frequency calculation of clock signal which determine the data transfer rate through cascade system. **10**
   (b) Explain EEPROM using floating gate NMOSFET. **10**

5. (a) Give various important parameters affecting switching performance of CMOS circuit. Suggest method to improve it. **10**
   (b) Give and explain single phase clock system and explain its drawback. **10**

[TURN OVER

6. (a) Explain various techniques of clock generation and clock stabilization. **10**

(b) What is cross talk in IC's? Explain various methods to reduce it. **10**

7. Write short notes on (any **three**) **20**

(a) Frequency compensation in CMOS operational amplifier.

(b) MODL.

(c) H tree clock distribution.

(d) Reliability issues in CMOS circuits
